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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,182	02/26/2002	Sadatoshi Narazaki	03500.016230	2431

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EXAMINER	
LIANG, LEONARD S	
ART UNIT	**PAPER NUMBER**
2853	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/082,182	NARAZAKI ET AL.	
	Examiner	Art Unit	
	Leonard S Liang	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification and Drawings

1. The lengthy specification and drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification and drawings.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 6-7, 11-13, 15, 17-18, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Cole et al (US Pat 5163153).

Cole et al discloses:

- {claim 1} a CPU having plural modes including a mode to reduce power consumption by suspending a clock signal as an operational mode, and receiving a signal from power switching means as an NMI interrupt signal for the execution of an NMI interrupt process (abstract; column 1, lines 27-52; figure 1A, reference 226; column 3, lines 55-65); non-volatile memory means for retaining a power supply status flag (column 3, lines 57-62); user logic circuit means for outputting a trigger signal, a mask signal generating portion for receiving the trigger signal to generate an NMI interrupt mask signal (figure 1,

reference 212; abstract); a gate circuit for making the signal from the power switching means invalid by the mask signal (abstract; figure 1A, reference 240; column 4, lines 4-25); control means for intiating operation of the recording apparatus in accordance with the flag at the time of the execution of the NMI interrupt process by the input of the signal from the power switching means, changing the flag, changing the operational mode of the CPU, and setting the user logic circuit means to prohibit the NMI interrupt until the operation is completed, and enabling the user logic circuit means to output the trigger signal in accordance with the setting, and the mask signal generating portion to generate the mask signal for making the signal from the power switching means invalid (figure 1A; abstract; column 3, line 39-column 4, line 25)

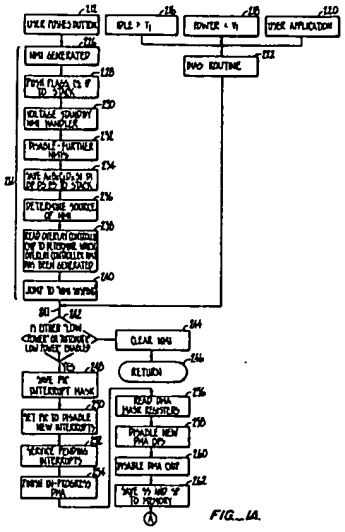


FIG. 1A.

- {claim 2} if the flag is ON, the power supply OFF is operated as the operation to change the flag to OFF, and as the operational mode change of the CPU, the

clock signal is suspended and the mode is changed to the mode for reducing the power consumption (figure 1A, reference 212, 226; column 3, lines 55-65)

- {claim 4} if the flag is OFF, the power supply ON is operated as the operation to change the flag to ON, and as the operational mode change of the CPU, the clock signal is suspended and the mode is changed from the mode for reducing power consumption (figure 1A, reference 212, 226; column 4, lines 26-42)
- {claim 6} a CPU having plural modes including a mode to reduce the power consumption by suspending a clock signal as an operational mode, and executing an NMI interrupt process with input of a signal from power switching means as an NMI interrupt signal (abstract; column 1, lines 27-52; figure 1A, reference 226; column 3, lines 55-65); abnormality detection means for detecting an abnormality (column 4, lines 4-16); user logic circuit means for outputting a trigger signal, a mask signal generating portion for receiving the trigger signal to generate an NMI interrupt mask signal (figure 1, reference 212; abstract); a gate circuit for making the signal from the power switching means invalid by the mask signal (abstract; figure 1, reference 240; column 4, lines 4-25); control means for setting the prohibition of the NMI interrupt for the user logic circuit means in accordance with an abnormal signal from the abnormality detection means, and outputting the trigger signal in accordance with the setting to enable the mask signal to be output from the mask signal generating portion to the gate circuit in accordance with the output trigger signal for making the signal from the

power switching means invalid (abstract; figure 1A; column 3, line 39-column 4, line 25)

- {claim 7} second abnormality detection means, wherein the gate circuit further executes a logical operation of an abnormal signal from the second abnormality detection means (column 3, line 39-column 4, line 25; inherent because multiple NMI's can be disabled which implies multiple aberrations or "abnormalities" which are detected and executed)
- {claim 11} a CPU having plural modes including a mode to reduce the power consumption by suspending a clock signal as an operational mode, and input means for inputting a signal from power switching means as an NMI interrupt signal for executing an NMI interrupt process (figure 1A, reference 226; abstract; column 1, lines 27-52; column 3, lines 55-65); user logic circuit means for outputting a trigger signal, a mask signal generating portion for receiving the trigger signal to generate an NMI interrupt mask signal (figure 1, reference 212; abstract); a gate circuit for making the signal from the power switching means invalid by the mask signal (abstract; figure 1, reference 240; column 4, lines 4-25); control means for setting the prohibition of the NMI interrupt for the user logic circuit means when the NMI interrupt signal is inputted by the input means for a designated number of times subsequent to the NMI interrupt process executed by the input of the signal from the power switching means, and enabling the user logic circuit means to output the trigger signal in accordance with the setting, and the mask signal generating portion to generate the mask

signal in accordance with the output of the trigger signal for making the signal from the power switching means invalid (figure 1; abstract; column 3, line 39-column 4, line 25)

- {claim 12} a CPU having plural modes including a mode to reduce power consumption by suspending a clock signal as an operational mode, and executing an NMI interrupt process with input of a signal from power switching means as an NMI interrupt signal (figure 1A; abstract; column 1, lines 27-52; column 3, line 39-column 4, line 25); retaining a power supply status flag in non-volatile memory means (column 3, lines 57-62); outputting a trigger signal from user logic circuit means and generating a mask signal in an NMI interrupt signal generating portion for NMI interrupt when the trigger signal is received (figure 1, reference 212; abstract); an operational process is executed in accordance with the flag retained in the flag retaining step when the NMI interrupt process is executed by the signal from the power switching means, and the flag retained in the flag retaining step is updated in the trigger signal outputting step for outputting the trigger signal in accordance with the setting for the user logic circuit, and the mask signal is generated in the mask signal generating step in accordance with the trigger signal for making the signal from the power switching means invalid by the generation of the mask signal until the operational process is completed (figure 1A; abstract; column 3, line 39-column 4, line 25)

- {claim 13} if the flag is ON, the operational process is an operational process of power supply OFF, and the flag is changed to suspend the clock signal as the operational mode change of the CPU for changing the mode to the mode for reducing power consumption (figure 1A, reference 212, 226; column 3, lines 55-65)
- {claim 15} if the flag is OFF, the operational process is an operational process of power supply ON, and the flag is changed to suspend the clock signal as the operational mode change of the CPU for changing the mode from the mode for reducing the power consumption (figure 1A, reference 212, 226; column 4, lines 26-42)
- {claim 17} a CPU having plural modes including a mode to reduce power consumption by suspending a clock signal as an operational mode, and executing an NMI interrupt process with input of a signal from power switching means as an NMI interrupt signal (figure 1; abstract; column 1, lines 27-52; column 3, lines 55-65); detecting an abnormality by abnormality detection means (column 4, lines 4-16); retaining a power supply status flag in non-volatile memory means (column 3, lines 57-62); outputting a trigger signal from user logic circuit means, and generating a mask signal in an NMI interrupt signal generating portion for NMI interrupt when the trigger signal is received (figure 1, reference 212; abstract); the abnormality is detected in the abnormality detecting step to output the trigger signal in the trigger signal outputting step in accordance with the abnormality, and the mask signal is generated in the mask signal generating step

in accordance with the output trigger signal for making the signal from the power switching means invalid by the generated mask signal (figure 1; abstract; column 3, line 39-column 4, line 25)

- {claim 18} a second abnormality detecting step for detecting an abnormality by second abnormality detection means, wherein the second abnormality detection means detects an abnormality, and the abnormality detection means outputs a signal (column 3, line 39-column 4, line 25; inherent because multiple NMI's can be disabled which implies multiple abnormalities are detected)
- {claim 22} a CPU having plural modes including a mode to reduce power consumption by suspending a clock signal as an operational mode, and input means for inputting a signal from power switching means as an NMI interrupt signal (abstract; column 1, lines 27-52; figure 1A, reference 226; column 3, lines 55-65); deciding whether or not the NMI interrupt signal is inputted into the input means a designated number of times; outputting a trigger signal from user logic circuit means; and generating a mask signal in an NMI interrupt signal generating portion for NMI interrupt by receiving the trigger signal, wherein an NMI interrupt prohibition is set for user logic circuit means when the input of the NMI interrupt signal is made in the designated number of times in the deciding step subsequent to the NMI interrupt process executed by the input of signal from the power switching means, the trigger signal is output in the trigger signal outputting step in accordance with the setting to the user logic circuit means for generating the mask signal in the mask signal generating step in accordance the

output of the trigger signal (figure 1A; abstract; column 3, line 39-column 4, line 25)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 5, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cole et al (US Pat 5163153) in view of Kanbayashi et al (EP Pat 0782924 A1).

Cole et al discloses:

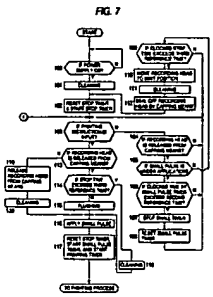
- {claims 3 and 5} an ink jet recording apparatus (as applied to claims 2 and 4)
- {claims 14 and 16} a method for controlling an ink jet recording apparatus (as applied to claims 13 and 15)

Cole et al differs from the claimed invention in that it does not disclose:

- {claims 3 and 14} the power supply OFF operation includes the capping operation to protect the recording head mounted on the ink jet recording apparatus
- {claims 5 and 16} the power supply ON operation includes the recovery operation for recovering the recording head mounted on the ink jet recording apparatus

Kanbayashi et al discloses:

- {claims 3 and 14} the power supply OFF operation includes the capping operation to protect the recording head mounted on the ink jet recording apparatus (figure 7, reference 112; column 6, line 59 – column 7, line 9)



- {claims 5 and 16} the power supply ON operation includes the recovery operation for recovering the recording head mounted on the ink jet recording apparatus (figure 7, reference 100, 101)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teachings of Kanbayashi et al into the invention of Cole et al. The motivation for the skilled artisan in doing so is to gain the benefit of performing capping in order to prevent nozzle openings from being clogged up and then recovering from such an operation (abstract).

4. Claims 8, 9, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cole et al (US Pat 5163153) in view of Yoshimura et al (US Pat 5262872).

Cole et al et al discloses:

- {claims 8 and 9} an ink jet recording apparatus (as applied to claims 6-7)

- {claims 19 and 20} a method of controlling an ink jet recording apparatus (as applied to claims 17-18)

Cole et al differs from the claimed invention in that it does not disclose:

- {claim 8} the abnormality detection means detects the abnormal temperature rise of the recording head mounted on the ink jet recording apparatus
- {claim 9} the second abnormality detection means detects the excessive voltage of the power supply provided for the ink jet recording apparatus
- {claim 19} the abnormal temperature of the recording head mounted on the ink jet recording apparatus is detected in the abnormality detecting step
- {claim 20} the excessive voltage of the power supply provided for the ink jet recording apparatus is detected in the second abnormality step

Yoshimura et al discloses:

- {claim 8} the abnormality detection means detects the abnormal temperature rise of the recording head mounted on the ink jet recording apparatus (column 23, lines 41-67)
- {claim 9} the second abnormality detection means detects the excessive voltage of the power supply provided for the ink jet recording apparatus (column 27, lines 28-39)
- {claim 19} the abnormal temperature of the recording head mounted on the ink jet recording apparatus is detected in the abnormality detecting step (as taught in claim 8)

- {claim 20} the excessive voltage of the power supply provided for the ink jet recording apparatus is detected in the second abnormality step (as taught in claim 9)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teachings of Yoshimura et al into the invention of Cole et al. The motivation for the skilled artisan in doing so is to gain the benefit of being able to detect errors (abstract).

5. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cole et al (US Pat 5163153) in view of Kaneko et al (US Pat 5428379).

Cole et al discloses, with respect to claims 10 and 21, an ink jet recording apparatus (as applied to claim 1) and a method for controlling an ink jet recording apparatus (as applied to claim 12).

Cole et al differs from the claimed invention in that it does not disclose that the recording head is provided with a plurality of recording members including an electrothermal converting element for generating thermal energy as energy for discharging ink.

Kaneko et al discloses, with respect to claims 10 and 21, the recording head is provided with a plurality of recording members including an electrothermal converting element for generating thermal energy as energy for discharging ink (column 3, lines 17-23).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the electrothermal converting element disclosed by Kaneko et

al into the invention of Cole et al. The motivation for the skilled artisan in doing so is to gain the benefit of generating thermal energy as energy for discharging ink (column 3, lines 17-23).

Response to Arguments

6. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miyazaki et al (US Pat 5933581) disc a communication apparatus for controlling switching between a normal mode and a power saving mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonard S Liang whose telephone number is (703) 305-4754. The examiner can normally be reached on 8:30-5 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Meier can be reached on (703) 308-4896. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

lsl LSL

LAMSON NGUYEN
PRIMARY EXAMINER
11/16/03